IN THE CLAIMS:

Claim 1-12. (Withdrawn)

Claim 13. (Currently Amended) A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components provided on a circuit surface, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a plurality of first electrodes provided in the first wiring layer; and

a second electrode provided on each of the conductive lines, each conductive line being configured to interconnect the plurality of first electrodes and the second electrode,

wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other.

Claim 14. (Currently Amended) A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components provided on a circuit surface, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a first electrode provided in the first wiring layer; and

a plurality of second electrodes provided on each of the conductive lines, the conductive lines being configured to interconnect the first electrode and the plurality of second electrodes,

wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other.

Claim 15. (Currently Amended) A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components provided on a circuit surface, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a plurality of first electrodes provided in the first wiring layer; and

a plurality of second ~~electrode~~ electrodes provided on each of the conductive lines, the conductive lines being configured to interconnect the plurality of first electrodes and the plurality of second electrodes,

wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other.

Claims 16-25. (Withdrawn)

Claim 26. (Original) The semiconductor apparatus according to claim 13, wherein the conductive lines form a large-size bus.

Claim 27. (Original) The semiconductor apparatus according to claim 13, wherein the conductive lines form a bus that interconnects the circuit components of the semiconductor apparatus.

Claim 28. (Original) The semiconductor apparatus according to claim 13, wherein one of the first and second chips includes external connection electrodes, the external connection electrodes being disposed in peripheral portions of said one of the first and second chips which do not interfere with the other of the first and second chips.

Claims 29-41. (Withdrawn)